

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 2001281303
PUBLICATION DATE : 10-10-01

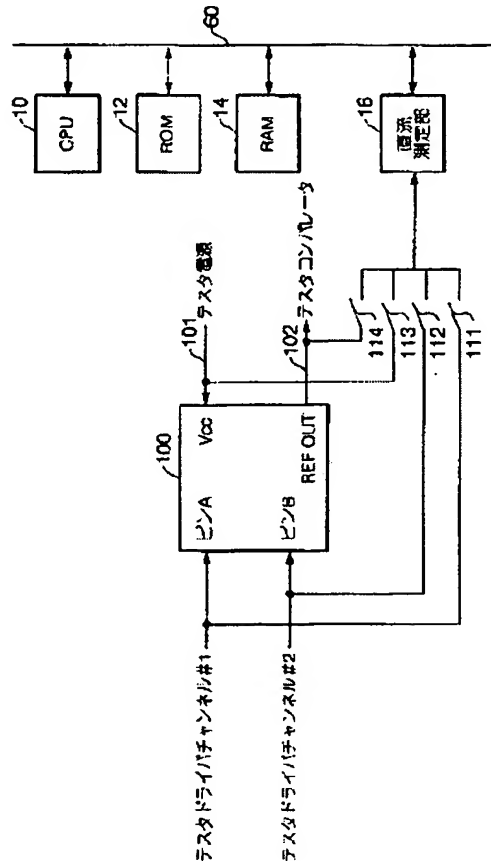
APPLICATION DATE : 28-03-00
APPLICATION NUMBER : 2000089816

APPLICANT : YAMAHA CORP;

INVENTOR : IIDA SHUNICHI;

INT.CL. : G01R 31/28 G01R 31/26 G01R 31/316
G01R 35/00

TITLE : SEMICONDUCTOR INTEGRATED
CIRCUIT TESTING DEVICE,
CALIBRATION METHOD FOR IT, AND
RECORDING MEDIUM



ABSTRACT : PROBLEM TO BE SOLVED: To suppress a relative error of a voltage set value fed to each pin of a measured device within the resolution range of a measurement system.

SOLUTION: The semiconductor integrated circuit testing device is provided with a common-use direct current measurement part 16 measuring an actual voltage value, which is fed from a specific related circuit in the semiconductor integrated circuit testing device connected to respective pins of a measured device 100 to the respective pin, for every pin during inspection of the measured device, a ROM 12 storing a voltage preset value fed to each pin of the measured device during the inspection time, and a CPU 10 finding an error between a voltage measurement value measured by means of the direct current measurement part 16 and fed to each pin and the preset value for every pin, performing feedback so that a voltage value having the opposite polarity to the error polarity and serving as a correction value is impressed to a pin having an error above an allowance value in the measured device and setting a supply voltage so as to lower the error below the allowance value.

COPYRIGHT: (C)2001,JPO